PENDING CLAIMS AND STATUS THEREOF

Claims 1-26 (canceled)

27. (original) A digital system adapted for serial digital data communications, said system comprising:

a transmitter and a receiver, said transmitter being adapted for sending serially encoded digital information and said receiver being adapted for receiving serially encoded digital information;

a computer adapted for serial digital data communications;

an event detector comprising:

a first bistable memory device, said bistable memory device having an input adapted for detecting the occurrence of an event and an output representing a logic state of said bistable memory device, wherein said logic state is at either a first or a second logic level such that the logic level of said logic state changes each time the event is detected;

a second bistable memory device, said bistable memory device having an input adapted for detecting the occurrence of an event and an output representing a logic state of said bistable memory device, wherein said logic state is at either a first or a second logic level such that the logic level of said logic state changes each time the event is detected; and

a digital processor, said digital processor having an input coupled to the output of said first bistable memory device and another input coupled to the output of said second bistable memory device, whereby said digital processor periodically reads said logic states and stores the logic levels thereof, wherein said

digital processor compares the logic level of a subsequently read logic state with the stored logic level so as to determine whether the stored logic level is the same or different than the logic level of said subsequently read logic state, if different then an event has occurred and if the same then no event has occurred;

wherein said event detector is coupled between said transmitter said computer, and said receiver and said computer such that said first bistable memory device is coupled to said receiver and said second bistable memory device is coupled to a serial output of said computer.

28. (original) The digital system of claim 27, wherein the transmission of said transmitter is selected from the group consisting of infrared, ultraviolet, radio frequency, microwave and ultrasonic.

29. (original) The digital system of claim 27, wherein the reception of said receiver is selected from the group consisting of infrared, ultraviolet, radio frequency, microwave and ultrasonic.

30. (original) The digital system of claim 27, wherein said computer is selected from the group consisting of a microcontroller, microprocessor, digital signal processor, reduced instruction set computer (RISC), complex instruction set computer (CISC).